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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,862	GUPTA ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on January 18, 2006. This amendment has been entered and carefully considered. Claims 1, 14-18, 22, 24, 27, 30 and 33 have been amended; and claim 26 has been newly added. Therefore, claims 1-36 are currently pending in this application.

2. Applicant's arguments filed on January 20, 2006 have been fully considered but they are not deemed to be persuasive.

3. The rejection of claims 1-35 as in the previous Office Action is respectfully maintained and reiterated below for Applicant's convenience.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

The phrase "... an upper-level system ..." should be written as "... the upper-level system ..." in claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 3-36 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kashima et al. (USPN: 5,485,598) hereinafter, Kashima.

As per claim 36, Kashima teaches a method comprising maintaining a first cache (i.e. the disk cache 13 in Fig. 4) and a second cache (i.e. old data cache 17 in Fig. 4), wherein said maintaining is performed by an upper-level system (i.e. the main memory 12 in Fig. 4); cloning (i.e. copying) information stored in a first unit of storage (the first cache memory 13 in Fig. 4) into a second unit of storage (the second cache memory 17 in Fig. 4) prior to modifying said information stored in said first unit of storage, wherein said first cache comprises said first unit of storage and said second cache comprises said second unit of storage; and providing access to said second cache by the other of said upper-level system and said lower-level system (i.e. by the CPU 11 in Fig. 4) (e.g. see the abstract and Fig. 4).

As per claim 1, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the first cache (i.e. the disk cache 13 in Fig. 4) is maintained by the upper-level system (i.e. the main memory 12 in Fig. 4) (e.g. see the abstract and Fig. 4).

As per claim 3, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said cloning comprises copying said information from said first unit of storage to said second unit of storage (e.g. see the abstract).

As per claim 4, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising:

- partially writing a unit of storage (i.e. a portion of data from the first cache) of a storage unit (i.e. the first cache) by writing a portion of said information (i.e. a portion of data from the first cache) from said second unit of storage (i.e. a portion of data from the second cache) to said unit of storage of said storage unit; and
- partially writing said unit of storage of said storage unit by writing new information (i.e. renewed data of the first cache) to said unit of storage of said storage unit (e.g. see the abstract).

As per claim 5, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said copying comprises:

- reading said information (i.e. the old data of the first cache) from said first unit of storage (i.e. the first cache); and
- writing said information (i.e. the old data of the first cache) to said second unit of storage (i.e. the second cache) (e.g. see the abstract).

As per claim 6, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising writing to said unit of storage after said reading, i.e. the old data is written/stored into the second cache after being read from the first cache (e.g. see the abstract).

As per claim 7, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising:

- reading said information (i.e. the old data) from said second unit of storage (i.e. from the second cache); and

- calculating parity information using said information, i.e. calculating new CK/parity data using the old data, the new data and the new CK data (e.g. see the abstract).

As per claims 8 and 9, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising:

- determining if said first unit of storage (the first cache) is to be modified, i.e. the new data to be written to the first cache; and
- performing said cloning (i.e. copying) if said first unit of storage is to be modified, i.e. if determined that the new data needs to be written to the first cache, then copying the old/existing data from the first cache into the second cache (e.g. see the abstract).

As per claim 10, see arguments with respect to the rejection of claim 7. Claim 10 is also rejected based on the same rationale as the rejection of claim 10.

As per claims 11 and 12, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising modifying said first unit of storage after said performing said cloning, i.e. writing new data into the first cache after copying old data from the first cache into the second cache (e.g. see the abstract).

As per claim 13, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said cloning comprising determining if said information will be needed in the future; and performing said cloning if said information will be needed in the future, i.e. if the old data is going to be renewed by the new data in

the first cache, then cloning/copying process is performed since the old data may be needed in future if the new data is lost/corrupted for any reason(s) (e.g. see the abstract).

As per claim 14, Kashima teaches a storage system (shown in Fig. 4) comprising an old data cache (i.e. old data cache 17 in Fig. 4), wherein said old data cache is configured to be maintained by an upper-level system (i.e. main memory 12 in Fig. 4) by the other of said upper-level system and said lower-level system (i.e. by the CPU 11 in Fig. 4) (e.g. see the abstract and Fig. 4).

As per claim 15, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the system further comprising:

- the upper-level system (i.e. 12 in Fig. 4) is communicatively coupled to said old data cache (i.e. 17 in Fig. 4); and
- the lower-level system (i.e. the disk array device, 1 in Fig. 4), communicatively coupled to said old data cache and said upper-level system (e.g. see Fig. 4).

As per claim 16, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level system is a volume manager (i.e. the RAID disk array, 1 in Fig. 8).

As per claim 17, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level system comprises a cache (i.e. the old CK data cache, 16 in Fig. 8).

As per claim 18, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level system is configured to clone/copy information from a page in said cache (i.e. the old CK data cache, 16 in Fig. 8) to a page in said old data cache (i.e. 17 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 19, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system (i.e. 12 in Fig. 4) is configured to access said page in said old data cache (i.e. 17 in Fig. 8).

As per claim 20, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system comprises a cache (i.e. the disk cache, 13 in Fig. 8).

As per claim 21, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system is configured to clone/copy information from a page in said cache (i.e. the disk cache, 13 in Fig. 8) to a page in said old data cache (i.e. 17 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 22, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level system (i.e. the disk array device, 1 in Fig. 8) is configured to access said page in said old data cache (i.e. 17 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 23, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system is a hardware RAID

controller since RAID (i.e. 1 in Fig. 8) is controlled by the upper-level system (i.e. the main memory, 12 in Fig. 8, specifically the CPU, 11 in Fig. 8) (e.g. see Fig. 8).

As per claim 24, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the system further comprising storage unit (i.e. disks, 2a-2d in Fig. 8), wherein said lower-level system (i.e. 16 in Fig. 8) is coupled to control said storage unit (e.g. see fig. 8).

As per claim 25, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the system further comprising a parity cache (i.e. the old CK data cache, 16 in Fig. 8), wherein said storage unit is a RAID (i.e. 2a-2d in Fig. 8), and said parity cache is configured to store parity information corresponding to data read from said RAID (e.g. see the claim 18).

As per claim 26, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said storage unit (i.e. the main memory, 12 in Fig. 8) comprises a source volume (i.e. 17 in Fig. 8) and a snapshot volume (i.e. 13 in Fig. 8), and said lower-level storage module (i.e. 1 in Fig. 8) is configured to write information from a page in said old data cache (i.e. 17 in Fig. 8) to said snapshot volume (i.e. 13 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 30, Kashima teaches a storage system comprising:

- a processor (i.e. the CPU 11 in Fig. 8);
- computer readable medium coupled to said processor; and computer code, encoded in said computer readable medium, configured to cause said

processor to, (i.e. this feature is inherently embedded in the system taught by Kashima):

- clone/copy information stored into a first unit of storage (the first cache) into a second unit of storage (the second cache), wherein
  - said first unit of storage is stored in a first cache (i.e. 17 in Fig. 8) maintained by an upper-level system (i.e. 12 in Fig. 8), and
  - said second unit of storage is stored in a second cache (e.g. see Fig. 8 and the abstract).

As per claim 31, see arguments with respect to the rejection of claims 30 and 4. Claim 31 is also rejected based on the same rationale as the rejection of claims 30 and 4.

As per claim 32, see arguments with respect to the rejection of claims 30 and 5-6. Claim 32 is also rejected based on the same rationale as the rejection of claims 30 and 5-6.

As per claims 27-29, see arguments with respect to the rejection of claims 30-32, respectively. Claims 27-29 are also rejected based on the same rationale as the rejection of claims 30-32, respectively.

As per claims 33-35, see arguments with respect to the rejection of claims 30-32, respectively. Claims 33-35 are also rejected based on the same rationale as the rejection of claims 30-32, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kashima.

As per claim 2, Kashima teaches the claimed invention as described above. Furthermore, Kashima also teaches that the main memory (i.e. 12 in Fig. 8) comprise the first and second caches (i.e. 13 and 17 in Fig. 8). However, Kashima does not clearly disclose that the first and second caches are a single cache. The common knowledge or well-known in the art statement, for the prior art teaching a single cache comprising a plurality of caches, is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)). First of all, it has been held that to make integral is not generally given patentable weight. Note In re Larson 144 USPQ 347 (CCPA 1965). Furthermore In re Tomoyuki Kohno 157 USPQ 275 (CCPA 1968) states that to integrate electrical components onto a unitary, one piece structure would be obvious. Integrating multiple components on a single chip reduces cabling problems, reduces latency required for communicating among multiple components, improves efficiency of message passing, reduces chip-to-chip communications costs, allows for less pin count, area saving and high speed data transfer between the elements and leads to further power efficiency and increased scalability. Because multiple caches integrated on a

single cache (chip) provides improvements in efficiency, cost and scalability over individual caches, it would have been obvious to comprise a plurality of caches on a single cache. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

Remarks

7. As to the remark, Applicant asserted that

(a) Old data cache 17 of Kashima is not configured to be maintained by one of an upper-level system and a lower-level system, and accessed by the other of the upper-level system and the lower-level system, as recited in claim 14.

(b) Applicants urge the Examiner to recognize the distinction between Applicants' claimed cloning operations and the common copying operations of Kashima.

(c) Kashima failed to provide features comparable to the claimed cloning, which is performed prior to information in the first unit of storage being modified, a first unit of storage being maintained by one of an upper-level system and a lower-level system, and second unit of storage being accessed by the other of the upper-level system and the lower-level system.

(d) Kashima fails to show the cloning of the first cache into the second cache prior to modifying information in the first cache.

(e) The copying of Kashima is obviously different than Applicants' claimed cloning and fails to anticipate Applicants' claimed cloning because neither of Kashima's first and second caches that are maintained by the upper-level system are accessed by a lower-level system.

(f) The Examiner has failed to address modifying Kashima in an attempt to support the cloning required by independent claim 36. Thus, no appropriate suggestion or motivation has been offered to modify Kashima as required to support a prima facie case of obviousness.

(g) Any modification to Kashima to show the cloning would not be based on Kashima's teachings or suggestion, but on Applicants' disclosure, which is improper hindsight.

(h) Kashima does not teach the features of claim 36 much less the single cache feature of dependent claim 2, and the features would not be obvious because the caching arrangement is irrelevant as to whether the upper-level system and the lower-level system access cloned information in a second cache or a single cache holding the cloned information.

(i) Kashima does not teach or suggest the limitations of dependent claim 2 because there is no advantage for Kashima to modify their invention in the manner of the claimed invention

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), the old data cache (i.e. 15 in Fig. 4) of Kashima is configured to be maintained by one of an upper-level system and a lower-level system (i.e. by the upper-level system 12 in Fig. 4), and accessed by the other of the upper-level system and the lower-level system (i.e. by the CPU 11 in Fig. 4) as recited in claim 14 (e.g. see Fig. 4).

With respect to (b), Examiner would like to point out to Applicant that the paragraphs [0069] and [0070] of the specification of the current application pointed out by Applicant does not define the "cloning process". Instead, the paragraph [0069] is explaining "a process for caching parity information corresponding to a cloned page" with reference to Fig. 5; and the paragraph [0070] is explaining "a process for writing a page to an old data cache" with reference to Fig. 6. Therefore, Applicant's argument regarding the distinction between Applicants' claimed cloning operations and the common copying operations of Kashima is rendered moot.

With respect to (c) and (d), Kashima does teach that the cloning (i.e. copying) process is performed prior to information in the first unit of storage (i.e. 13 in Fig. 4) being modified, a first unit of storage being maintained by one of an upper-level system (i.e. 12 in Fig. 4) and a lower-level system, and second unit of storage (i.e. 1 in Fig. 4) being accessed by the other of the upper-level system and the lower-level system (i.e. 11 in Fig. 4) (e.g. see the abstract and Fig. 4).

With respect to (e), Kashima's first cache (i.e. the data cache 13 in Fig. 4) is maintained by the upper-level system (i.e. by the main memory 12 in Fig. 4) is accessed by a lower-level system (i.e. the disk array 1 in Fig. 4) (e.g. see Fig. 4).

With respect to (f) and (g), the claim 36 is rejected based on 35 USC 102(b) as shown above. Therefore, Applicants' arguments regarding modification to Kashima, supporting a prima facie case of obviousness, improper hindsight etc. are rendered moot.

With respect to (h), claim 36 is clearly anticipated by Kashima reference as shown above in the rejection of claim 36. As per claim 2, Kashima does teach the claimed invention including that the main memory (i.e. 12 in Fig. 8) comprise the first and second caches (i.e. 13 and 17 in Fig. 8). However, Kashima does not clearly disclose that the first and second caches are a single cache. The common knowledge or well-known in the art statement, for the prior art teaching a single cache comprising a plurality of caches, is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)).

With respect to (i), Kashima teaches the computer (i.e. 10 in Fig. 8) having the main memory (i.e. 12 in Fig. 8) that comprises the first and second caches (i.e. 13 and 17 in Fig. 8) (e.g. see Fig. 8). However, Kashima does not clearly disclose that the first and second caches are a single cache. Integrating multiple components on a single chip reduces cabling problems, reduces latency required for communicating among multiple components, improves efficiency of message passing, reduces chip-to-chip communications costs, allows for less pin count, area saving and high speed data transfer between the elements and leads to further power efficiency and increased scalability. Because multiple caches integrated on a single cache (chip) provides

improvements in efficiency, cost and scalability over individual caches, it would have been obvious to comprise a plurality of caches on a single cache. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW D. ANDERSON
PRIMARY EXAMINER